1. A method of controlling the slew rate on the output terminal of an output buffer wherein the current delivered to said output terminal is varied during voltage transitions of said output terminal.

2. The method according to Claim 1 wherein said variation of said current delivered to said output terminal during said voltage transitions of said output terminal is accomplished by:

sequentially turning on a plurality of n first conducting devices when said voltage transition of said output terminal is from a first voltage level to a second voltage level thereby connecting said output terminal to a first fixed voltage potential; and

sequentially turning on a plurality of m second conducting devices when said voltage transition of said output terminal is from said second voltage level to said first voltage level thereby connecting said output terminal to a second fixed voltage potential wherein said second fixed voltage potential is less than said first fixed potential.

3. The method according to Claim 2 wherein said first conducting devices are PMOS transistors.

4. The method according to Claim 2 wherein said second conducting devices are NMOS transistors.

5. The method according to Claim 2 wherein said sequentially turning on said plurality of n first conducting devices is accomplished by turning on of each of said first conducting devices after a delay such that the first of said plurality of first conducting devices has the shortest said delay and subsequent conducting devices have subsequently longer said delays.

6. The method according to Claim 5 wherein the time duration of said delay is controlled by a network comprising resistance and capacitance.

7. The method according to Claim 6 wherein said capacitance is comprised of the combination of parasitic capacitance of said first conducting device and a first feedback device.

8. The method according to Claim 7 wherein said first feedback device is an NMOS transistor.

9. The method according to Claim 2 wherein said sequentially turning on said plurality of m second conducting devices is accomplished by turning on of each of said second conducting devices after a delay such that the first of said plurality of second conducting devices has the shortest said delay and subsequent conducting devices have subsequently longer said delays.

10. The method according to Claim 9 wherein the time duration of said delay is controlled by a network comprising resistance and capacitance.

11. The method according to Claim 10 wherein said capacitance is comprised of the combination of parasitic capacitance of said second conducting device and a second feedback device.

12. The method according to Claim 11 wherein said second feedback device is a PMOS transistor.

13. A device for controlling the slew rate on the output terminal of an output buffer wherein the rising transition of the voltage on said output terminal is achieved by sequentially activating a plurality of n distinct pull-up current driver stages each comprised of:

a pull-up signal input terminal;

a pull-up device which when activated will electrically connect said output terminal to a first fixed voltage potential;

a pull-up delay circuit which, when an activating signal is presented to said pull-up signal input terminal, will activate said pull-up device after a pull-up time delay;

a pull-up feedback device which when activated will feedback a portion of the signal on said output terminal to the input of said pull-up device;

a pull-up enabling device which when activated with an enable signal will activate said pull-up feedback device;

and wherein the falling transition of said voltage on said output terminal is achieved by sequentially activating a plurality of m distinct pull-down current driver stages each comprised of:

a pull-down signal input terminal;

a pull-down device which when activated will electrically connect said output terminal to a second fixed voltage potential;

a pull-down delay circuit which, when an activating signal is presented to said pull-down signal input terminal, will activate said pull-down device after a pull-down time delay;

a pull-down feedback device which when activated will feedback a portion of said signal on said output terminal to the input of said pull-down device; and

a pull-down enabling device which when activated with an enable signal will activate said pull-down feedback device.

14. The device according to Claim 13 wherein said pull-up device is a PMOS transistor.

15. The device according to Claim 13 wherein said pull-down device is an NMOS transistor.

16. The device according to Claim 13 wherein said pull-up delay device is comprised of a resistance and capacitance and wherein the duration of said pull-up time delay is controlled by selecting the values of said resistance and said capacitance.

17. The device according to Claim 16 wherein said capacitance is comprised of the combination of parasitic capacitance of said pull-up device and said pull-up feedback device.

18. The device according to Claim 13 wherein said pull-down delay device is comprised of a resistance and capacitance and wherein the duration of said pull-down time delay is controlled by selecting the values of said resistance and said capacitance.

19. The device according to Claim 18 wherein said capacitance is comprised of the combination of parasitic capacitance of said pull-down device and said pull-down feedback device.

20. The device according to Claim 13 wherein said pull-up feedback device is an NMOS transistor.

21. The device according to Claim 13 wherein said pull-down feedback device a PMOS transistor.

22. The device according to Claim 13 wherein said pull-up enabling device is an NMOS transistor.

23. The device according to Claim 13 wherein said pull-down enabling device a PMOS transistor.

24. A device for controlling the slew rate on the output terminal of an output buffer wherein the rising transition of the voltage on said output terminal is achieved by sequentially activating a plurality of n distinct pull-up current driver stages each comprised of:

a pull-up signal input terminal;

a PMOS transistor which when activated will electrically connect said output terminal to a first fixed voltage potential;

a pull-up delay circuit which, when an activating signal is presented to said pull-up signal input terminal, will activate said PMOS transitor after a pull-up time delay;

a pull-up feedback device which when activated will feedback a portion of the signal on said output terminal to the gate of said PMOS transitor; and

a pull-up enabling device which when activated with an enable signal will activate said pull-up feedback device;

wherein the falling transition of said voltage on said output terminal is achieved by sequentially activating a plurality of m distinct pull-down current driver stages each comprised of:

a pull-down signal input terminal;

an NMOS transistor which when activated will electrically connect said output terminal to a second fixed voltage potential;

a pull-down delay circuit which, when an activating signal is presented to said pull-down signal input terminal, will activate said NMOS transistor after a pull-down time delay;

a pull-down feedback device which when activated will feedback a portion of said signal on said output terminal to the gate of said NMOS transistor; and

a pull-down enabling device which when activated with an enable signal will activate said pull-down feedback device.

25. The device according to Claim 24 wherein said pull-up delay device is comprised of a resistance and capacitance and wherein the duration of said pull-up time delay is controlled by selecting the values of said resistance and said capacitance.

26. The device according to Claim 25 wherein said capacitance is comprised of the combination of parasitic capacitance of said PMOS transistor and said pull-up feedback device.

27. The device according to Claim 24 wherein said pull-down delay device is comprised of a resistance and capacitance and wherein the duration of said pull-down time delay is controlled by selecting the values of said resistance and said capacitance.

28. The device according to Claim 27 wherein said capacitance is comprised of the combination of parasitic capacitance of said NMOS transistor and said pull-down feedback device.

29. The device according to Claim 24 wherein said pull-up feedback device is an NMOS transistor.

30. The device according to Claim 24 wherein said pull-down feedback device a PMOS transistor.

31. The device according to Claim 24 wherein said pull-up enabling device is an NMOS transistor.

32. The device according to Claim 24 wherein said pull-down enabling device a PMOS transistor.